

Correlation between charge trap distribution and memory characteristics in metal/oxide/nitride/oxide/silicon devices with two different blocking oxides, Al₂O₃ and SiO₂

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We examined the origin of the charge traps in both SiO₂/Si₃N₄/SiO₂ (ONO) and Al₂O₃/Si₃N₄/SiO₂ (ANO) structures and their effect on the memory characteristics by capacitance-voltage (*C-V*) measurements and deep level transient spectroscopy (DLTS). A larger memory window was observed by *C-V* for ANO, due to its higher trap density. The DLTS showed that nitride traps are dominant in ANO, while more Si/SiO₂ interface-related traps are observed in ONO. The ANO capacitor outperforms the ONO one in terms of both the program efficiency and retention, which is attributed to the reduced number of interface traps in ANO. © 2008 American Institute of Physics. [DOI: 10.1063/1.2970990]

The polycrystalline silicon-oxide-nitride-oxide-silicon (SONOS) structure has attracted a great deal of attention for the next generation of flash memory applications, because of its advantages such as its film scalability, process simplicity, and power economy. However, as the nitride thickness and the gate size are reduced to the nanometer scale, charges are trapped close to the gate electrode and most of them are lost through it, resulting in data loss.^{1,2} In order to solve the problems involved in the device scaling for sub 100 nm flash technology nodes, a high- κ material has been applied as a blocking oxide layer. Al₂O₃ has been considered one of the attractive candidates for the blocking oxide among the high- κ materials that have been studied so far^{3,4} because it features a large energy band gap of 8.7 eV, a large conduction band offset of 2.8 eV with respect to silicon, and a large dielectric constant of 9. In fact, most of the reports on high- κ studies have been focused on improving the device performance, without any detailed investigation of the trap distributions, which determine the memory characteristics in charge-trap type devices, across the Al₂O₃/Si₃N₄/SiO₂ (ANO) structures in comparison with those of the SiO₂/Si₃N₄/SiO₂ (ONO) structure.

In this letter, we investigate the distribution of charge traps across the ONO and ANO structures and its effect on the memory characteristics by capacitance-voltage (*C-V*) measurements and deep level transient spectroscopy (DLTS).

For this experiment, we prepared two types of samples, viz., metal/silicon-oxide/nitride/oxide/silicon and metal/aluminum-oxide/nitride/oxide-silicon (MANOS) capacitors, having the same electrical thickness in the layer structures, by using a thicker blocking oxide layer of Al₂O₃ than that of SiO₂. The thickness of the ONO film was 65/60/20 Å, and that of the ANO film was 150/60/20 Å. A tunnel oxide layer was grown by thermal oxidation. Then a nitride layer was deposited by low-pressure chemical vapor deposition (CVD). Next, a blocking layer of SiO₂ was deposited for the

ONO stack using high-temperature oxide CVD at ~900 °C while an Al₂O₃ blocking layer was deposited for the ANO stack using an atomic layer deposition technique at ~500 °C. The thickness of the Al₂O₃ layer was chosen to be 150 Å, thus making it electrically equivalent to that of the top SiO₂ layer when considering the dielectric constant and physical thickness of Al₂O₃. It is important to have the same electric field applied to the tunnel oxide layers for each of the samples while investigating the trap distributions, in order to eliminate the influence of the electric field.

Figure 1 shows the *C-V* hysteresis curves at the critical bias points for the ONO and ANO structures grown on *p*-type Si. We found that a leakage current was produced in the ONO and ANO capacitors under bias sweeping conditions of more than 10 and 20 V, respectively. At this point, the maximum flatband shifts were typically ~505 V for the ONO capacitor and ~18 V for the ANO capacitor, as shown in Fig. 1. The flatband voltage shift ΔV_{FB} is known to be proportional to the spatial trapped charge density N_T (cm⁻³). This relation is given as follows:⁵

$$\Delta V_{FB} = \frac{qN_T X_N}{\epsilon_{OX}} \left(X_{OB} + \frac{\epsilon_{OX} X_N}{2\epsilon_N} \right), \quad (1)$$

where X_N is the thickness of the Si₃N₄ layer, X_{OB} is the thickness of the blocking oxide (SiO₂ or Al₂O₃), ϵ_N is the

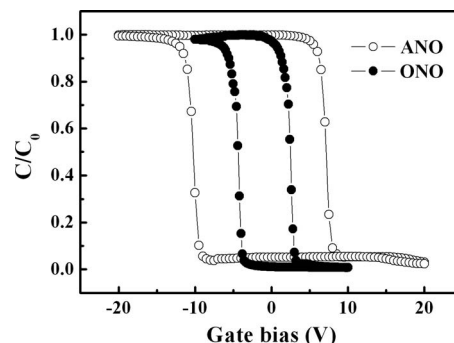


FIG. 1. *C-V* hysteresis curves at the critical bias point for the ONO and ANO structures grown on *p*-type Si.

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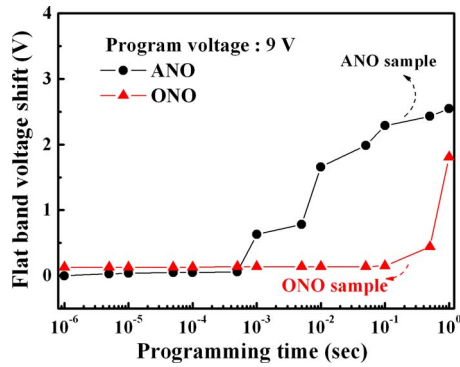


FIG. 2. (Color online) The program characteristics measured for both the ONO and ANO structures, where the ΔV_{FB} was plotted against the program time.

dielectric constant of Si_3N_4 , and ϵ_{OX} is the dielectric constant of the blocking oxide. To calculate the charge density trapped spatially in Si_3N_4 , we defined the maximum flatband voltage shift in the case of both the full program and full erase states. In our experiment, the trapped charge density of ONO was calculated from Eq. (1) to be 2.42×10^{19} ($/\text{cm}^3$) and that of ANO was 7.92×10^{19} ($/\text{cm}^3$). This result indicates that more physical trap sites are available for the ANO structure than for the ONO one.

We then investigated the program efficiencies of the two samples by measuring the program speed and ΔV_{FB} . Figure 2 shows the program efficiency of the ONO and ANO structures where ΔV_{FB} was plotted against the program time. For the program time of 50 ms, for example, the ΔV_{FB} of the ANO capacitor was close to 2 V, while only a small value of ΔV_{FB} was observed for the ONO capacitor. This result indicates that the program efficiency of the ANO structure is much higher than that of the ONO structure. This improved efficiency of the ANO structure is thought to be associated with the trap energy levels in the nitride layer. Chen *et al.*⁶ reported that the memory traps in the shallow energy levels of the nitride layer allowed the electrons to be more readily injected from the substrate, eventually improving the program efficiency. Since the ANO structure has more memory traps in relatively shallow energy levels under the same bias conditions, it would be expected to be able to be charged (or programmed) faster than the ONO one.

In order to verify this feature, we calculated the distribution of the trap density in the energy levels of the Si_3N_4 layer using a charge decay model, which was proposed for SONOS by Kim *et al.*⁷ Using this model, the distribution of the electron trap density can be estimated at elevated temperatures (>150 °C) with respect to the energy level of the Si_3N_4 in retention mode. Figure 3 shows the trap density distribution in the energy level of the ONO and ANO structures extracted using the charge decay model. In Fig. 3, we find that the trap density of ANO is higher than that of ONO in the lower energy levels (below 1.25 eV), indicating that more traps are located in the shallower energy levels in the ANO structure than in the ONO one. In this measurement, the read delay time was limited to the range from 1 to 10^5 s, which corresponds to the scanning range of the trap energy from 0.8 to 1.3 eV below the conduction band minimum of Si_3N_4 , in order to increase the credibility of the data on the shallow level traps. Above 10^5 s (or 1.3 eV), it seems that the charge decay model is no longer reliable, since the elec-

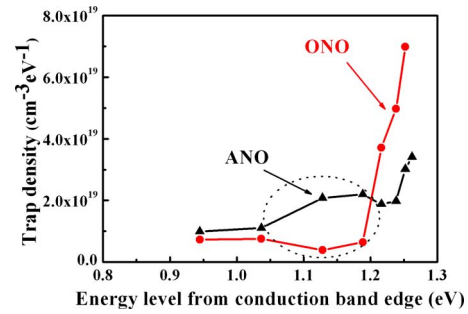


FIG. 3. (Color online) Trap density distribution in the energy level of the ONO and ANO structures extracted using a charge decay model.

tron traps are so deeply located in the band gap that the electrons cannot be readily activated by thermal excitation.⁹ In any case, this result is in good agreement with those presented in Fig. 2. Therefore, we attribute the improved program efficiency of the MANOS capacitor to the fact that the trap distributions are dominantly located in the shallow energy levels of the ANO structure.

However, these deep level traps cannot be analyzed by the charge decay model. So, we used DLTS to investigate the spatial distribution of the memory traps that may be present in the deep level regions of the ONO and ANO structures. We prepared two samples, ONO and ANO, grown on *n*-type Si substrates to characterize the electron memory traps. Figure 4 shows the DLTS spectra for the ONO and ANO structures fabricated on the *n*-type Si substrates. In our previous work,¹⁰ DLTS analysis was conducted for the *n*-type ONO structure, where two electron traps were observed at the locations of 180 K (denoted as n_{p1}) and 320 K (n_{p2}), respectively. These peaks were attributed to the nitride traps (traps related to the nitride layer) and interfacial traps (traps related to the interface between Si and SiO_2), respectively. Similarly, we observed two DLTS peaks near 200 K n_{p1} and 300 K n_{p2} , respectively, from the ANO structure. However, interestingly, the ONO and ANO structures exhibited opposite behavior in terms of the peak intensity. That is, n_{p2} representing the interface trap density was dominantly observed in the ONO structure, while n_{p1} representing the nitride trap density was mainly observed in the ANO structure. The peak intensity of DLTS is proportional to the trap density. Consequently, the ANO structure has relatively more nitride traps and less Si-SiO₂ interface traps in the deep energy levels.

Figure 5 shows the flatband voltage shifts versus read delay time for the ANO and ONO structures at room temperature. The average charge decay rate of ANO is 0.18

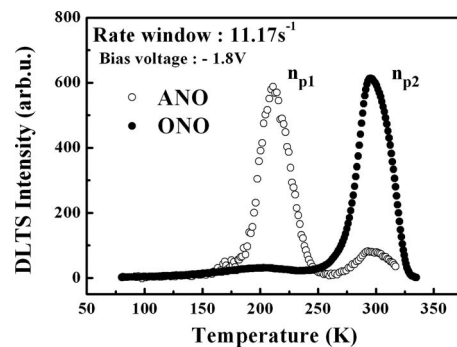


FIG. 4. DLTS spectra measured from ONO and ANO capacitors fabricated on *n*-type Si substrates.

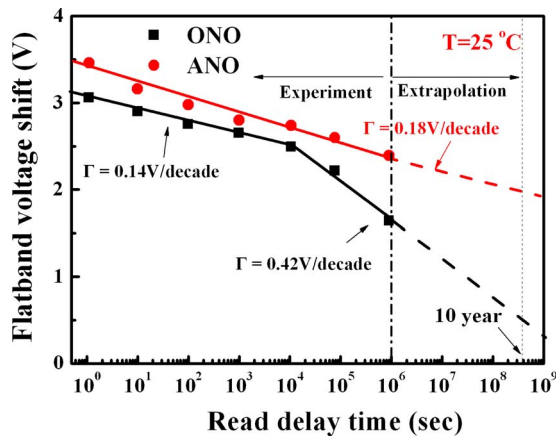


FIG. 5. (Color online) Retention characteristics of the ONO and ANO structures at room temperature, showing the relationship between the flatband voltage shift and read delay time.

V/decade in the written state. Then, the flatband voltage shift was extrapolated against the read delay time to predict the long-term retention of the ANO, and found to be 2.0 V at 3×10^8 s (or 10 years). On the other hand, it appears that the ONO structure is not suitable for 10-year retention applications, because its charge decay rate is 0.15 V/decade, which is less than that of the ANO below 10^4 s. However, it increases rapidly to as high as 0.42 V/decade above 10^4 s. This kind of long-term retention problem has been pointed out in SONOS devices.^{8,11} Because the charges are trapped efficiently at the deep trap centers, the ANO structure, having a larger trap density in the deep energy levels as well as a thicker blocking oxide, is thought to have better retention properties than ONO, especially in terms of the long-term stability. Moreover, it is important to reduce the interface traps between Si and SiO₂, as much as possible, as observed in the ANO structure, because this could be a factor that can degrade the device reliability (or retention).^{12,13} Regarding the physical origin of the larger trap density in the ANO structure, it might be related to the interface traps between the blocking oxide and the nitride layer, since all the deposition processes are the same except for the blocking layers. Further investigation is required to identify it.

In summary, *C-V* and DLTS analyses were conducted for both ONO and ANO capacitors to investigate the energy distribution of the charge traps and its effect on the memory characteristics in these devices. Through the *C-V* analyses, we found that the ANO structure would have a larger memory window than the ONO one, due to its higher trap density. In addition, the DLTS analyses, with a charge decay model, showed that nitride traps were dominant for ANO in both the shallow and deep energy levels, while Si/SiO₂ interface traps were dominant for ONO. The ANO capacitor outperformed the ONO one in terms of both the program efficiency and retention, which was attributed to the reduced number of interface traps as well as the ideal trap distributions across the ANO structures. These results show that the ANO structure, even with a physically thicker blocking oxide, is still more suitable than ONO for application to charge-trap memory devices.

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